REMARKS

The Examiner rejected claims 1, 4, 7, 12-14 and 20 under 35 U.S.C. §103(a) as allegedly being unpatentable over Adams *et al.* (USPN 5535164) further in view of Applicants' Admitted Prior Art (AAPA).

Applicants respectfully traverse the §103(a) rejections with the following arguments.

35 U.S.C. §103(a)

The Examiner rejected claims 1, 4, 7, 12-14 and 20 under 35 U.S.C. §103(a) as allegedly being unpatentable over Adams *et al.* (USPN 5535164) further in view of Applicants' Admitted Prior Art (AAPA).

Applicants respectfully contend that claims 1, 4, 7, 12-14, and 20 are not unpatentable over Adams further in view of AAPA, because Adams further in view of AAPA does not teach or suggest each and every feature of claims 1, 4, 7, 12-14, and 20 .

As a first reason why claims 1, 4, 7, 12-14, and 20 are not unpatentable over Adams further in view of AAPA, Adams further in view of AAPA does not teach or suggest the following first feature of a "plurality of memory arrays, each memory array comprising a compilable address magnitude comparator". The preceding first feature of claim 1 is shown in Applicants' specification on page 8, lines 11-13 and is illustrated in FIG. 1 of Applicants' patent application which depicts compilable address magnitude comparators 106 and 108 as being comprised by memory arrays 102 and 104, respectively.

The Examiner argues that CAM 24 in FIG. 1 of Adams is a comparator. However, Adams teaches a single CAM 24 which is located **external** to the memories 12, 14, 16, 18, and 20 of FIG. 1, and therefore does not satisfy the preceding feature of claim 1, namely "each memory array **comprising** a compilable address magnitude comparator" (emphasis added).

In Response to Arguments, the Examiner argues: "Adams teaches (Figure 5 and associated text) a plurality of memory arrays, each memory away comprising a compilable address magnitude comparator. The Examiner would like to point out, with regards to Applicable arguments that the CAM is located external to the memories, that Adams teaches a BIST, which shows that the CAMS to be internal as can be seen in Figure 5 as well".

In response, Applicants respectively contend that the comparators 170, 172, 174, and 176 in FIG. 5 are located **external** to the memory arrays comprised by the 64x16 bit CAM, and therefore does not satisfy the preceding feature of claim 1, namely "each memory array **comprising** a compilable address magnitude comparator" (emphasis added).

Therefore Adams does not teach or suggest the preceding first feature of claims 1, 4, 7, 12-14, and 20.

As a second reason why claims 1, 4, 7, 12-14, and 20 are not unpatentable over Adams further in view of AAPA, the Adams further in view of AAPA does not teach or suggest the following second feature: "the compilable address magnitude comparator of each memory array receiving a self-test address from a self-test controller".

Applicants maintain that neither CAM 24 in FIG. 1 nor the comparators 170, 172, 174, and 176 in FIG. 5 perform receiving a self-test address from a self-test controller, as required by claims 1, 4, 7, 12-14, and 20.

As a third reason why claims 1, 4, 7, 12-14, and 20 are not unpatentable over Adams further in view of AAPA, the Adams further in view of AAPA does not teach or suggest the following third feature: "the compilable address magnitude comparator of each memory array ... comparing the self-test address to a compiled maximum address of each memory array".

Applicants maintain that neither CAM 24 in FIG. 1 nor the comparators 170, 172, 174, and 176 in FIG. 5 perform the address comparisons required in the preceding feature of claims 1, 4, 7, 12-14, and 20. Indeed, the CAM 24 in FIG. 1 and the comparators 170, 172, 174, and 176 in FIG. 5 compare only data patterns and most certainly do not compare addresses. See Adams col. 4, line 57 - col. 5, line 13; col. 14, line 57 -col. 15, line 13. Only the BIST makes address comparisons in Adams. See Adams, col. 3, lines 26-29 ("BIST 10 shuts off each memory's WE and LR signals as the current address exceeds that memory's address space and whenever else appropriate according to the individual memory's function.").

Therefore Adams does not teach or suggest the preceding third feature of claims 1, 4, 7, 12-14, and 20.

As a fourth reason why claims 1, 4, 7, 12-14, and 20 are not unpatentable over Adams further in view of AAPA, the Adams further in view of AAPA does not teach or suggest the following fourth feature: "the compilable address magnitude comparator of each memory array preventing testing of memory of each memory array corresponding to the self-test address if the self-test address exceeds the compiled maximum address of each memory array." Applicants maintain that Adams does not disclose that any of the comparators (i.e., CAM 24 in FIG. 1; comparators 170, 172, 174, and 176 in FIG. 5) perform preventing testing of memory of each memory array corresponding to the self-test address. In other words, the comparators in Adams perform comparing but do not perform "preventing testing of memory of each memory array corresponding to the self-test address".

Therefore Adams does not teach or suggest the preceding fourth feature of claims 1, 4, 7, 12-14, and 20.

As a fifth reason why claims 1, 4, 7, 12-14, and 20 are not unpatentable over Adams further in view of AAPA, the Adams further in view of AAPA does not teach or suggest the following fifth feature: "wherein the compilable address magnitude comparator of each memory array prevents testing of memory of each memory array by forcing a memory pass signal". The Examiner does not even allege that Adams further in view of AAPA teaches or suggests the preceding fourth feature of claims 1, 4, 7, 12-14, and 20.

Therefore Adams does not teach or suggest the preceding fifth feature of claims 1, 4, 7, 12-14, and 20.

As a sixth reason why claims 1, 4, 7, 12-14, and 20 are not unpatentable over Adams further in view of AAPA, the Adams further in view of AAPA does not teach or suggest the following sixth feature: "wherein the compilable address magnitude comparator of each memory array includes a row comparator and a column comparator, the row comparator comparing a self-test row address of each memory array and the column comparator comparing a self-test column address of each memory array". The Examiner does not even allege that Adams further in view of AAPA teaches or suggests the preceding sixth feature of claims 1, 4, 7, 12-14, and 20.

Therefore Adams does not teach or suggest the preceding sixth feature of claims 1, 4, 7, 12-14, and 20.

Moreover, Applicants respectfully traverse the Examiner's arguments for modifying Adams to include a compilable address magnitude comparator.

The Examiner admits: "Adams does not explicitly teach the address comparator to be a "compilable address magnitude comparator" as stated in the present application."

The Examiner argues: "However, the specification on the present application teaches (specification, pages 1-4), in part, the compilable magnitude comparator address comparator overrides the self-test from the BIST when the BIST attempts to test addresses that do not exist in the memory. The Examiner would like to point that Adams teaches, as previously stated, a single BIST which can test various memories of different sizes, types and characteristics, wherein the BIST shuts off each memory's WE and LR signals as the current address exceeds that memory's address space and whenever else appropriate according to the individual memory's function. Shutting off the WE prevents rewriting memory locations through a particular pattern. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Adams by incorporating a `compilable address magnitude comparator" within the method and apparatus. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would lave recognized that by making the address magnitude compilable would enable it to efficiently override the self-test from the BIST when the BIST attempts to test addresses that do not exist in the memory" (emphasis added).

In response, Applicants respectfully contend that the Examiner's reliance on pages 1-4 of Applicants' specification is misdirected, because pages 1-4 of Applicants' specification does not disclose that "the compilable magnitude comparator address comparator overrides the self-test from the BIST when the BIST attempts to test addresses that do not exist in the memory", as alleged and relied upon by the Examiner. In fact, the word "comparator" does not appear anywhere in pages 1-4 of Applicants' specification. Applicants respectfully request that the Examiner identify where and how pages 1-4 of Applicants' specification "teaches ... , in part, the compilable magnitude comparator address comparator overrides the self-test from the BIST when the BIST attempts to test addresses that do not exist in the memory. "

Accordingly, Applicants maintain that AARP cannot be used as a basis for modifying Adams.

Based on the preceding arguments, Applicants respectfully maintain that claims 1, 4, 7, 12-14, and 20 are not unpatentable over Adams further in view of AAPA, and that claims 1, 4, 7, 12-14, and 20 are in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner ton contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account No. 09-0456.

Date: 11/28/2005

Jack P. Friedman
Registration No. 44,688

Schmeiser, Olsen & Watts
3 Lear Jct Lane, Suite 201
Latham, New York 12110
(518) 220-1850